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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,325	07/28/2003	Larry R. Tate	042390.P15891	6608

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EXAMINER	
TU, JULIA P	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,325	TATE ET AL.	
	Examiner	Art Unit	
	Julia P. Tu	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed December 24, 2003 fails to comply with 37 CFR 1.98(a)(1), which requires the following: (1) a list of all patents, publications, applications, or other information submitted for consideration by the Office; (2) U.S. patents and U.S. patent application publications listed in a section separately from citations of other documents; (3) the application number of the application in which the information disclosure statement is being submitted on each page of the list; (4) a column that provides a blank space next to each document to be considered, for the examiner's initials; and (5) a heading that clearly indicates that the list is an information disclosure statement. The information disclosure statement has been placed in the application file, but the information referred to therein has not been considered.

Drawings

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4, 7-11, 12-15, 18-22, 23-26, 29-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Terashima et al. (US 2003/0043926).

(1) with regard to claim 1:

As shown in figures 3 and 4, Terashima et al. disclose a method comprising:

establishing at least two sequences of predetermined reference times (n clocks in figures 3 and 4) on respective ones of at least two communication lines (n communication lines in figure 3), at least some of the reference times of at least one of the sequences occurring out-of-phase with at least some of the reference times of another of the sequences (CLK0, CLK1, CLKn are out of phase in figure 4), and

encoding digital data (i.e. coding in figure 3) onto data signals on one or more communication lines such that a time difference between at least one of the data signals and the nearest one of the reference times on one of the communication lines is smaller

than the time difference between the same data signal and the nearest one of the reference times on another one of the communication lines (Transmitting end in figures 3 and 4; page 4, paragraphs [0071] and [0074]; figure 14, page 7, paragraphs [0104] and [0105]).

(2) with regard to claim 12:

As shown in figures 3 and 4, Terashima et al. disclose an apparatus comprising:

a source of at least two reference signals, each containing a sequence of predetermined reference times (n clocks in figures 3 and 4), at least some of the reference times of at least one of the sequences occurring out-of-phase with at least some of the reference times of another of the sequences (CLK0, CLK1, CLKn are out of phase in figure 4);

a modulator circuit having one or more outputs for data signals (200-20n and 110-11n in the transmitting end of figure 3) onto which digital data have been encoded such that a time difference between at least one of the data signals and the nearest one of the reference times on one of the reference signals is smaller than the time difference between the same data signal and the nearest one of the reference times on another one of the reference signals, and at least two outputs for the reference signals (Transmitting end in figures 3 and 4; page 4, paragraphs [0071] and [0074]; figure 14, page 7, paragraphs [0104] and [0105]).

a demodulator circuit with at least one input for the data signals and at least two inputs for the reference signals (see receiving end in figures 3 and 4).

a data bus comprising communication lines (130-13n in figure 3) which are connected to both the modulator circuit and the demodulator circuit, which can enable the transmission of the data signals and the reference signals between the modulator and demodulator circuits.

(3) with regard to claim 23:

As shown in figures 3, 4, and 5, Terashima et al. disclose a system comprising at least two integrated circuits mounted on at least one circuit board;

a data bus (130-13n in figures 3, 4, and 5);

at least one modulator circuit (200-20n and 110-11n in the transmitting end of figure 3);

at least one demodulator circuit (see receiving end in figures 3 and 4);

a source of at least two reference signals, each containing a sequence of predetermined reference times (n clocks in figures 3 and 4), at least some of the reference times of at least one of the sequences occurring out-of-phase with at least some of the reference times of another of the sequences (CLK0, CLK1, CLKn are out of phase in figure 4);

the modulator circuit having one or more outputs for data signals (200-20n and 110-11n in the transmitting end of figure 3) onto which digital data have been encoded such that a time difference between at least one of the data signals and the nearest one of the reference times on one of the reference signals is smaller than the time difference between the same data signal and the nearest one of the reference times on another one of the reference signals, and at least two outputs for the reference signals

(Transmitting end in figures 3 and 4; page 4, paragraphs [0071] and [0074]; figure 14, page 7, paragraphs [0104] and [0105]).

the demodulator circuit (see receiving end in figures 3 and 4) with at least one input for the data signals and at least two inputs for the reference signals; and

the data bus comprising communication lines (130-13n in figures 3, 4, and 5) which are connected to both the modulator circuit and the demodulator circuit, which can enable the transmission of the data signals and the reference signals between the modulator and demodulator circuits.

(4) with regard to claims 2, 13, 24:

Terashima et al. further disclose the reference times are rising or falling transitions of digital signals (transmitting end in figure 4, page 4, paragraph 0074).

(5) with regard to claims 3, 14, 15:

Terashima et al. further disclose the data signals are at one of multiple potential time locations of rising or falling transitions of digital signals, where the multiple potential time locations comprise a data symbol (figure 4, page 4, paragraph [0074]).

(6) with regard to claims 4, 15, 26:

Terashima et al. further disclose encoding comprises associating a particular digital data value with one of the multiple potential rising transitions of the data symbol, and associating a particular digital data value with one of the multiple potential falling transitions of the data symbol (figure 4, page 4, paragraph [0074]).

(7) with regard to claims 7, 18, 29:

Terashime et al. further teach decoding the digital data based on the data signals and the sequences (receiving end in figure 3).

(8) with regard to claims 8, 19, 30:

Terashime et al. further teach decoding comprises delaying at least one of the sequences (receiving end in figures 3 and 5, page 5, paragraph [0081]).

(9) with regard to claims 9, 20, 31:

Terashime et al. further teach decoding comprises delaying at least one of the data signals (receiving end in figures 3 and 5, page 5, paragraph [0081]).

(10) with regard to claims 10, 21, 32:

Terashime et al. further teach decoding further comprises determining the order in time between one of the data signals and one of the reference times (page 4, paragraph [0074]; note in figure 5, the receiver send the signal back to the transmitter to determine the timing).

(11) with regard to claims 11, 22, 33:

The method of claim 10 where decoding the digital data is based on the order in time (page 4, paragraph [0074]).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 6, 16, 17, 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terashima et al. (US 2003/0043926) in view of Kim et al. (US 6,463,092).

(1) with regard to claims 5, 16, 27:

Terashima et al. further teach each of the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals.

However, as shown in figures 10A, 11 (A, B), and 12 (A, B), Kim et al. disclose the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals (see rising edge detector 1002 in figure 10A, column 12, lines 1-15, figures 11 and 12).

It is desirable to include the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals to control signaling between the transmitter and the receiver without decreasing the available bandwidth for data transfer as well as to reduce the latency in sending control signals (column 2, lines 1-4). Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to include the data signals comprises one of multiple potential amplitude levels between pre-determined time locations of rising or falling transitions of digital signals as taught by Kim et al. to the system as taught by Terashima et al. to enhance the processing time as well as the accuracy of the communication system.

(2) with regard to claims 6, 17, 28:

Kim et al. further teach encoding comprises associating a particular digital data value with one of the multiple potential amplitude levels (column 4, lines 29-33).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Synder et al. (US 5,910,742) disclose the circuit comprise a clock generator configured to generate a plurality of clocks and/or a logic circuit configured to select the clock signal having the closest timing relationship with the data signal.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Julia P. Tu whose telephone number is 571-270-1087. The examiner can normally be reached on 7:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

J.T.
11-26-2006

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER